

ABSTRACT

5 A 256 Meg dynamic random access memory is comprised of
a plurality of cells organized into individual arrays, with
the arrays being organized into 32 Meg array blocks, which
10 are organized into 64 Meg quadrants. Sense amplifiers are
positioned between adjacent rows in the individual arrays
while row decoders are positioned between adjacent columns
in the individual arrays. In certain of the gap cells,
multiplexers are provided to transfer signals from I/O lines
15 to data lines. A datapath is provided which, in addition to
the foregoing, includes array I/O blocks, responsive to the
datalines from each quadrant to output data to a data read
mux, data buffers, and data driver pads. The write data
path includes a data in buffer and data write muxes for
20 providing data to the array I/O blocks. A power bus is
provided which minimizes routing of externally supplied
voltages, completely rings each of the array blocks, and
provides gridded power distribution within each of the array
blocks. A plurality of voltage supplies provide the
25 voltages needed in the array and in the peripheral circuits.
The power supplies are organized to match their power output
to the power demand and to maintain a desired ratio of power
production capability and decoupling capacitance. A powerup
sequence circuit is provided to control the powerup of the
chip. Redundant rows and columns are provided as is the
circuitry necessary to logically replace defective rows and
columns with operational rows and columns. Circuitry is

